#16 Amdt. C
Shaver
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S/N 09/208,105 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	SAKAMOTO	Examiner:	O. NADAV
Serial No.:	09/208,105	Group Art Unit:	2811
Filed:	NOVEMBER 25, 1998	Docket No.:	10233.81USW1
Title:	SEMICONDUCTOR DEVICE WITH METAL WIRE LAYER MASKING (AS AMENDED HEREIN)		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited in the United States Postal Service, as first class mail, with sufficient postage, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on ~~February 28, 2001~~ April 2, 2001.

By: Pat Bradley
Name: PAT BRADLEY

AMENDMENT UNDER RULE 111

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Official Action dated September 29, 2000, please amend this application as follows:

In the Specification

Please change the title to -- SEMICONDUCTOR DEVICE WITH METAL WIRE LAYER MASKING--.

Please replace the paragraph beginning at page 1, line 18, with the following rewritten paragraph:

--A substrate 82 used for the IGBT 80 includes a drain layer 3 with P^+ type, an n^+ type layer 5 and an n^- type layer 7. Base regions 21 are formed in the n^- type layer 7, and source regions 23 with n^+ type are formed within the base regions 21. The surface of the n^- type semiconductor layer 82 is covered with a gate oxidation layer 22.--

Please replace the paragraph beginning at page 1, line 25, with the following rewritten paragraph:

--Incidentally, a loss caused by switching arises as a result of a parasitic diode generated on a plane of a PN (positive-negative) junction 59. Japanese Patent laid-open publication No.